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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,226	06/26/2000	Donald E. Steiss	TI-29338	3213

7590 06/17/2003

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,226	STEISS ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2000 and 25 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-18 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 19 August 2000; Declaration as received on 11 September 2000; and IDS as received on 25 July 2002.

Specification

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example**, please change page 1, lines 14-15 from "in each instruction. (a MultiOp instruction.) VLIW architectures are horizontal machines, with each wide instruction-word or *Multi*Op, consisting of several operations , *Ops*." to read -- in each instruction (a MultiOp instruction). VLIW architectures are horizontal machines, with each wide instruction-word, or *Multi*Op, consisting of several operations, *Ops*.-- Please clarify on page 1, lines 27 and 28 whether the phrases [4, 5, 3] and [18, 2, 14, 8, 7, 6] refer to reference elements or something pertaining to the specification. Please correct page 1, line 30 from "resources and the exact operation latencies permits highly optimized) schedules." to read -- resources and the exact operation latencies permits highly optimized schedules.--

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 3, 10, 12, and 16 are rejected under 35 U.S.C. 102(a) as being taught by Shiell et al., U.S. Patent Number 5,961,632 (herein referred to as Shiell).

6. Referring to claim 1, Shiell has taught the structure of a subpipelined translation embodiment providing binary compatibility between a base architecture and migrant architecture comprising:

a. A VLIW architecture (Shiell column 3, lines 36-42) comprising a base architecture and a migrant architecture and having a base execution mode and a migrant execution mode (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; and Figure 5);

b. A fetch packet retrieved from memory, the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

c. A shared datapath by both the base and migrant architectures for parsing said base architecture mode and migrant architecture mode fetch packets into execute packets and for dispatching those base execute packets to the appropriate base architecture decode of the execute hardware (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

d. A migrant architecture control circuit for dispatching execute packet instructions having a migrant execution mode to a migrant architecture decode (Shiell

Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

e. Execute hardware for executing execute packet instructions on execution units and having a base architecture decode and a migrant architecture decode for decoding said base architecture instructions and said migrant architecture instructions, respectively, in dependence upon the execution mode of the fetch packet of the instructions being decoded, prior to executing (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

f. A multiplexer having at least two inputs and one machine word output wherein one input is the output of said migrant architecture decode and the other input is the output of said base architecture decode, said multiplexer choosing in dependence upon the operating mode of said fetch packet (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

g. Machine words for controlling the execution hardware units (Shiell column 3, lines 25-35);

7. Referring to claim 3, Shiell has taught wherein said machine word also controls registers (Shiell column 3, lines 25-46).

8. Referring to claim 10, Shiell has taught a method of providing binary compatibility between a base architecture and migrant architecture comprising the steps of:

a. Executing a base execution mode and a migrant execution mode on a base architecture and a migrant architecture (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; and Figure 5), respectively, on a VLIW architecture (Shiell column 3, lines 36-42);

b. Providing a fetch packet retrieved from a memory, the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

c. Parsing said base architecture mode and migrant architecture mode fetch packets into execute packets and dispatching those base execute packets to the appropriate base architecture decode of the execute hardware on a shared datapath by both the base and migrant architectures (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

d. Dispatching execute packet instructions having a migrant execution mode to a migrant architecture decode on a migrant architecture control circuit (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

e. Executing execute packet instructions on execution units of execute hardware, said execute hardware having a base architecture decode and a migrant architecture decode for decoding said base architecture instructions and said migrant architecture instructions, respectively, in dependence upon the execution mode of the fetch packet of the instructions being decoded, prior to executing (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

f. Choosing, in dependence upon the operating mode of said fetch packet, between the output of said migrant architecture decode and the output of said base architecture decode in a multiplexer having one machine word output (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

g. Controlling the execution hardware units with said machine word (Shiell column 3, lines 25-45).

9. Referring to claim 12, Shiell has taught controlling registers with said machine word (Shiell column 3, lines 25-46).

10. Referring to claim 16, Shiell has taught translating opcodes to the control signals required to execute the specified instructions on the execution hardware functional units within the base and migrant architecture decode units (Shiell Abstract; column, line 61 to column 2, line 7;

column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 4-9, 11, 13-15, and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., U.S. Patent Number 5,961,632 (herein referred to as Shiell) in view of Nishioka et al., U.S. Patent Number 6,401,190 (herein referred to Nishioka).

13. Referring to claims 2, 4-9, Shiell has taught a VLIW architecture further comprising:

a. Wherein said machine word controls the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to said machine word controlling said local register files (Applicant's claim 6) (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5)

b. Wherein the base and migrant architecture decode units translates opcodes to the control signals required to execute the specified instructions on the execution hardware functional units (Applicant's claim 7) (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5)

14. Shiell has not explicitly taught a VLIW architecture further comprising:

a. A third input to said multiplexer wherein said third input is a no operation instruction (Applicant's claim 2);

b. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4);

c. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5);

d. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8); and

e. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9).

15. However, Shiell has taught that the VLIW instruction set architecture is one of many possible instructions sets that can be used in the device (Shiell column 3, lines 36-42), but not the explicit details of the VLIW instruction set architecture. Nishioka has taught explicitly a VLIW architecture (Nishioka column1, line 41 to column 2, line 4) further comprising:

a. A third input to said multiplexer wherein said third input is a no operation instruction (Applicant's claim 2) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6);

b. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4) (Nishioka column 4, lines 7-62);

c. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5) (Nishioka column 4, lines 7-62);

d. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6); and

e. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9) (Nishioka column 1, lines 14-41).

16. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture is advantageous over other instruction sets, because it simplifies hardware and how the hardware is controlled, since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

17. Referring to claims 11, 13-15, and 17-18, Shiell has taught a VLIW architecture method further comprising controlling the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to controlling said local register files (Applicant's claim 15) (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5).

18. Shiell has not explicitly taught a VLIW architecture method further comprising:

a. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11);

b. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13);

c. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14);

d. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17); and

e. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18).

19. However, Shiell has taught that the VLIW instruction set architecture is one of many possible instructions sets that can be used in the device (Shiell column 3, lines 36-42), but not the specific details of the VLIW architecture. Nishioka has taught explicitly a VLIW architecture method (Nishioka column1, line 41 to column 2, line 4) further comprising:

a. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5, and Figure 6);

b. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13) (Nishioka column 4, lines 7-62);

c. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14) (Nishioka column 4, lines 7-62);

d. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17) (Nishioka column 1, lines 14-41); and

e. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6).

20. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture is advantageous over other instruction sets, because it simplifies hardware and how the hardware is controlled, since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

21. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond et al., U.S. Patent Number 5,638,525 (herein referred to as Hammond) in view of Nishioka et al., U.S. Patent Number 6,401,190 (herein referred to Nishioka).

22. Referring to claims 1-9, Hammond has taught the structure of a subpipelined translation embodiment providing binary compatibility between a base architecture and migrant architecture comprising:

a. A base architecture and a migrant architecture and having a base execution mode and a migrant execution mode (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; and Figure 3);

b. A fetch packet retrieved from memory, the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

c. A shared datapath by both the base and migrant architectures for parsing said base architecture mode and migrant architecture mode fetch packets into execute packets and for dispatching those base execute packets to the appropriate base architecture decode of the execute hardware (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

d. A migrant architecture control circuit for dispatching execute packet instructions having a migrant execution mode to a migrant architecture decode (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

e. Execute hardware for executing execute packet instructions on execution units and having a base architecture decode and a migrant architecture decode for decoding said base architecture instructions and said migrant architecture instructions, respectively, in dependence upon the execution mode of the fetch packet of the instructions being decoded, prior to executing (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

f. A multiplexer having at least two inputs and one machine word output wherein one input is the output of said migrant architecture decode and the other input is the output of said base architecture decode, said multiplexer choosing in dependence upon the operating mode of said fetch packet (Applicant's claim 1)

(Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

g. Machine words for controlling the execution hardware units (Applicant's claim 1) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3). In regards to Hammond, machine words must be present in order for the device to properly execute.

h. Wherein said machine word also controls registers (Applicant's claim 3) (Hammond column 12, lines 41-49 and Figure 3);

i. Wherein said machine word controls the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to said machine word controlling said local register files (Applicant's claim 6) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3); and

j. Wherein the base and migrant architecture decode units translates opcodes to the control signals required to execute the specified instructions on the execution hardware functional units (Applicant's claim 7) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3).

23. Hammond has not explicitly taught

a. A VLIW architecture (Applicant's claim 1) further comprising:

i. A third input to said multiplexer wherein said third input is a no operation instruction (Applicant's claim 2);

ii. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4);

iii. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5);

iv. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8); and

v. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9).

24. However, Hammond has taught that instruction sets used may be any type of instruction sets, including 64 bit instructions (Hammond column 2, lines 1-17 and column 9, line 64 to column 10, line 4). It was well known to a person of ordinary skill in the art at the time this invention was made that 64 bits is a common size for VLIW instructions. Nishioka has explicitly taught

a. A VLIW architecture (Applicant's claim 1) (Nishioka column1, line 41 to column 2, line 4) further comprising:

i. A third input to said multiplexer wherein said third input is a no operation instruction (Applicant's claim 2) (Nishioka column 7, lines 31-59; column

8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6);

ii. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4) (Nishioka column 4, lines 7-62);

iii. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5) (Nishioka column 4, lines 7-62);

iv. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6); and

v. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9) (Nishioka column 1, lines 14-41).

25. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture is advantageous over other instruction sets, because it simplifies hardware and how the hardware is controlled, since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka

column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

26. Referring to claims 10-18, Hammond has taught a method of providing binary compatibility between a base architecture and migrant architecture comprising the steps of:

a. Executing a base execution mode and a migrant execution mode on a base architecture and a migrant architecture (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; and Figure 3);

b. Providing a fetch packet retrieved from a memory, the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

c. Parsing said base architecture mode and migrant architecture mode fetch packets into execute packets and dispatching those base execute packets to the appropriate base architecture decode of the execute hardware on a shared datapath by both the base and migrant architectures (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

d. Dispatching execute packet instructions having a migrant execution mode to a migrant architecture decode on a migrant architecture control circuit (Applicant's

claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

e. Executing execute packet instructions on execution units of execute hardware, said execute hardware having a base architecture decode and a migrant architecture decode for decoding said base architecture instructions and said migrant architecture instructions, respectively, in dependence upon the execution mode of the fetch packet of the instructions being decoded, prior to executing (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

f. Choosing, in dependence upon the operating mode of said fetch packet, between the output of said migrant architecture decode and the output of said base architecture decode in a multiplexer having one machine word output (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3);

g. Controlling the execution hardware units with said machine word (Applicant's claim 10) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3). In regards to Hammond, machine words must be present in order for the device to properly execute.

h. Controlling registers with said machine word (Applicant's claim 12) (Hammond column 12, lines 41-49 and Figure 3);

i. Controlling the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to controlling said local register files (Applicant's claim 15) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3); and

j. Translating opcodes to the control signals required to execute the specified instructions on the execution hardware functional units within the base and migrant architecture decode units (Applicant's claim 16) (Hammond Abstract, lines 1-5; column 1, lines 55-60; column 2, lines 1-17; column 11, line 64 to column 12, line 49; and Figure 3).

27. Hammond has not explicitly taught

a. A VLIW architecture (Applicant's claim 10) further comprising:

i. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11);

ii. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13);

iii. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14);

iv. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17); and

v. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18).

28. However, Hammond has taught that instruction sets used may be any type of instruction sets, including 64 bit instructions (Hammond column 2, lines 1-17 and column 9, line 64 to column 10, line 4). It was well known to a person of ordinary skill in the art at the time this invention was made that 64 bits is a common size for VLIW instructions. Nishioka has explicitly taught

a. A VLIW architecture (Applicant's claim 10) (Nishioka column1, line 41 to column 2, line 4) further comprising:

i. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5, and Figure 6);

ii. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13) (Nishioka column 4, lines 7-62);

iii. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14) (Nishioka column 4, lines 7-62);

iv. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17) (Nishioka column 1, lines 14-41); and

v. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6).

29. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture is advantageous over other instruction sets, because it simplifies hardware and how the hardware is controlled, since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of

claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Blomgren et al., U.S. Patent Number 5,884,057, has taught a system that decodes two separate, individual instruction sets.

b. Borrill, E.P. 0 709 767, has taught a VLIW architecture with multiple instruction sets and decoders.

c. Tremblay et al., WO 00/33178, has taught a VLIW system with local and global registers.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

33. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

June 16, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100